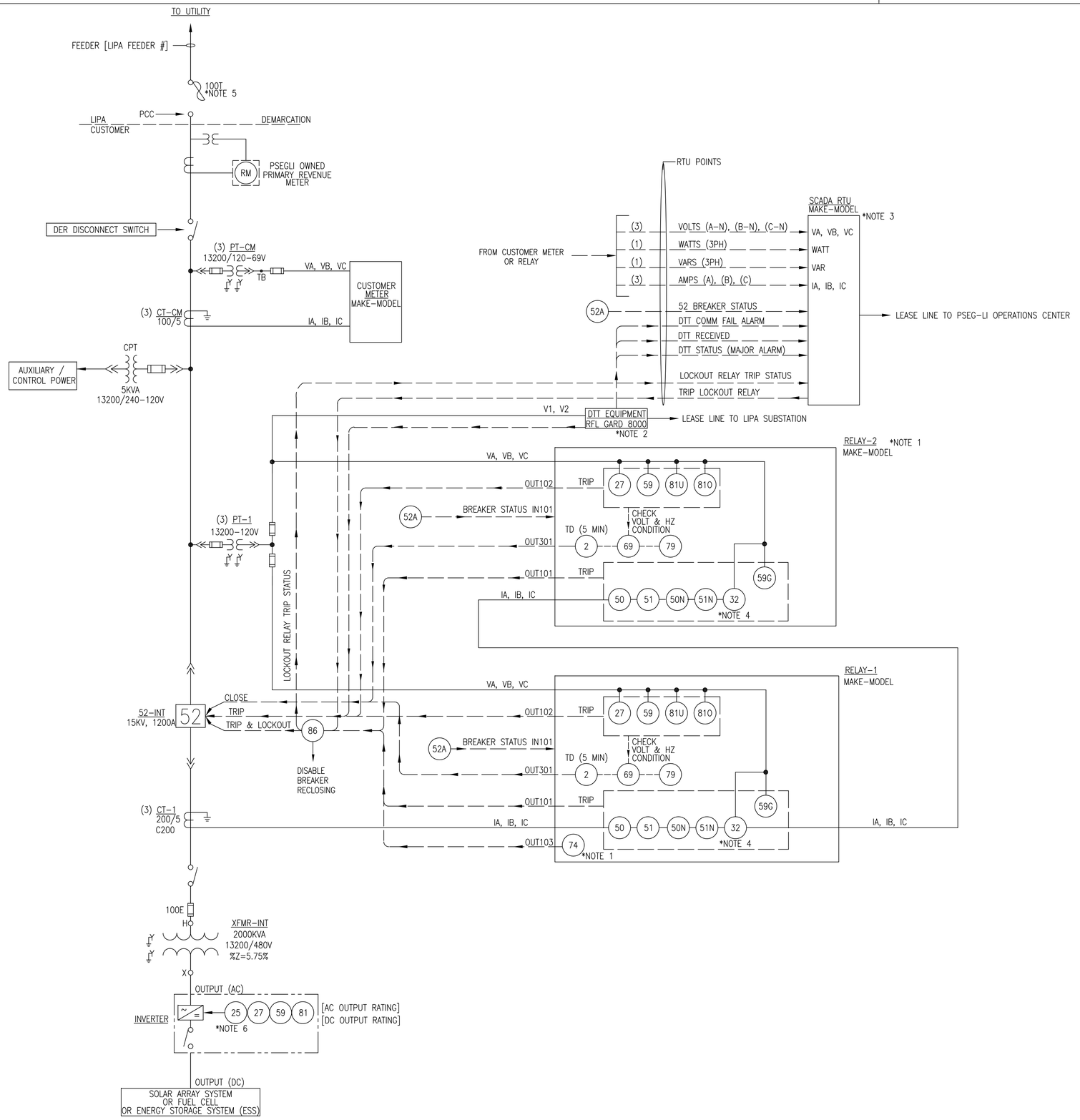


ANSI FUNCTIONS

- (2) TIME DELAY CLOSING RELAY
- (25) SYNCH CHECK RELAY
- (27) UNDERVOLTAGE RELAY
- (32) DIRECTIONAL POWER
- (50) PHASE INSTANTANENOUS OVERCURRENT RELAY
- (50N) GROUND INSTANTANEOUS OVERCURRENT RELAY
- (51) PHASE TIME OVERCURRENT RELAY
- (51N) GROUND TIME OVERCURRENT RELAY
- (52) CIRCUIT BREAKER
- (59) OVERVOLTAGE RELAY
- (59G) ZERO SEQUENCE OVER VOLTAGE (3V0)
- (69) PERMISSIVE CONTROL DEVICE
- (74) RELAY FAILURE ALARM
- (79) RECLOSING RELAY
- (81 U/O) UNDER/OVER FREQUENCY RELAY
- (86) LOCKOUT RELAY (MANUAL RESET)

INTEGRATED INVERTER SETTINGS			
VOLTAGE SETTINGS			
ANSI NO.	TRIP	PICKUP (%)	TIME DELAY (SEC)
27-1	UNDERVOLTAGE	SETTINGS AS PER LATEST SGIP GUIDE SECTION 8.5.4	
27-2	UNDERVOLTAGE		
59-1	OVERVOLTAGE		
59-2	OVERVOLTAGE		
FREQUENCY SETTINGS			
ANSI NO.	TRIP	PICKUP (HZ)	TIME DELAY (SEC)
81/U-1	UNDERFREQUENCY	SETTINGS AS PER LATEST SGIP GUIDE SECTION 8.5.4	
81/U-2	UNDERFREQUENCY		
81/O-1	OVERFREQUENCY		
81/O-2	OVERFREQUENCY		

NOTE 1: RELAY FAILURE TRIP IS NOT REQUIRED IF TWO REDUNDANT UTILITY GRADE RELAYS ARE USED

NOTE 2: IF DTT REQUIRED BY LIPA

NOTE 3: IF SCADA RTU REQUIRED BY LIPA

NOTE 4: DIRECTIONAL POWER RELAY (32) MAY BE REQUIRED TO LIMIT OR PREVENT EXPORT POWER FLOW TO CONTRACTUAL AGREEMENT

NOTE 5: ACTUAL FUSE SIZE TO BE DETERMINDED BY LIPA

NOTE 6: SYNCH CHECK RELAY (25) MUST BE SHOWN FOR GRID FORMING INVERTERS

THIS DRAWING IS AN EXAMPLE OF TYPICAL INTERCONNECTION TO ILLUSTRATE THE TYPE OF INFORMATION TO BE PROVIDED.
EACH PROJECT IS SITE SPECIFIC, MAY HAVE DIFFERENT REQUIREMENTS, RATINGS, SIZES, ETC.
DER OWNER/DEVELOPER IS RESPONSIBLE FOR EQUIPMENT RATINGS, SIZES AND FINAL CONFIGURATION.

ISSUE NO.	DATE	W.O.	DESCRIPTION	DWN BY	CKD BY	REVIEWED	APPD
4	2/2024		REVISE DTT SCHEME				
3	1/2023		REMOVE LOR RESET				
2	2/2022		CLARIFICATIONS				
1	9/2020		MINOR REVISIONS				
0	1/2019		ORIGINAL ISSUE				

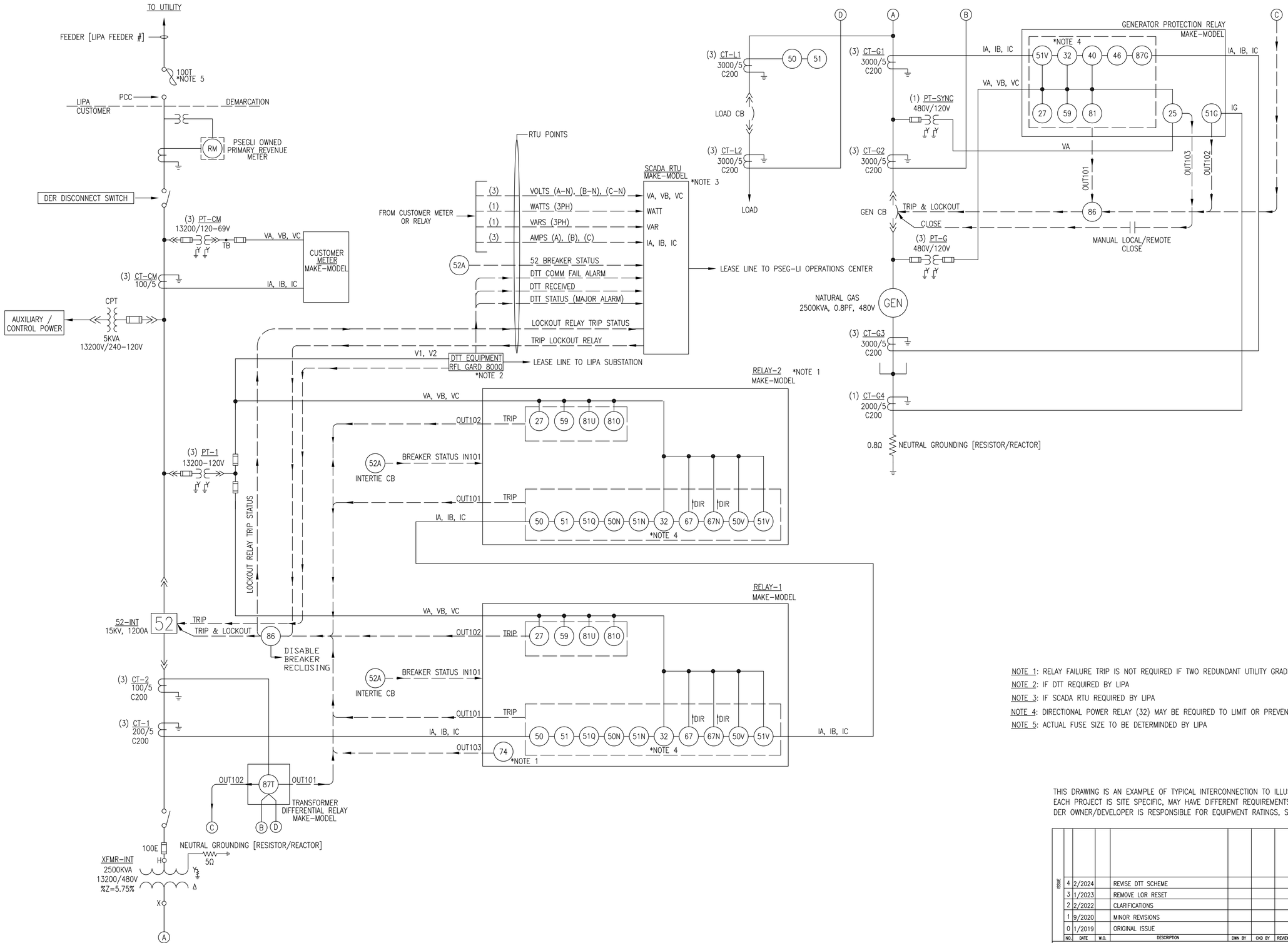
APPENDIX D
SAMPLE DRAWING D-1

FUNCTIONAL DIAGRAM
INVERTER BASED DER

PSEG LONG ISLAND

SCALE

VENDOR DWG. NO.



ANSI FUNCTIONS

- 25 SYNCH CHECK RELAY
- 27 UNDERVOLTAGE RELAY
- 32 DIRECTIONAL POWER
- 40 LOSS OF EXCITATION RELAY
- 50 PHASE INSTANTANENOUS OVERCURRENT RELAY
- 50N GROUND INSTANTANEOUS OVERCURRENT RELAY
- 50V VOLTAGE RESTRAINED PHASE INSTANTANEOUS RELAY
- 51 PHASE TIME OVERCURRENT RELAY
- 51G GENERATOR NEUTRAL TIME OVERCURRENT RELAY
- 51N GROUND TIME OVERCURRENT RELAY
- 46 / 51Q NEGATIVE SEQUENCE TIME OVERCURRENT RELAY
- 51V VOLTAGE RESTRAINED PHASE TIME OVERCURRENT RELAY
- 52 CIRCUIT BREAKER
- 59 OVERVOLTAGE RELAY
- 67 PHASE DIRECTIONAL OVERCURRENT
- 67N GROUND DIRECTIONAL OVERCURRENT RELAY
- 74 RELAY FAILURE ALARM
- 81 U/O UNDER/OVER FREQUENCY RELAY
- 86 LOCKOUT RELAY (MANUAL RESET)
- 87G GENERATOR DIFFERENTIAL RELAY
- 87T TRANSFORMER DIFFERENTIAL RELAY

NOTE 1: RELAY FAILURE TRIP IS NOT REQUIRED IF TWO REDUNDANT UTILITY GRADE RELAYS ARE USED

NOTE 2: IF DTT REQUIRED BY LIPA

NOTE 3: IF SCADA RTU REQUIRED BY LIPA

NOTE 4: DIRECTIONAL POWER RELAY (32) MAY BE REQUIRED TO LIMIT OR PREVENT EXPORT POWER FLOW TO CONTRACTUAL AGREEMENT

NOTE 5: ACTUAL FUSE SIZE TO BE DETERMINDED BY LIPA

THIS DRAWING IS AN EXAMPLE OF TYPICAL INTERCONNECTION TO ILLUSTRATE THE TYPE OF INFORMATION TO BE PROVIDED.
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DER OWNER/DEVELOPER IS RESPONSIBLE FOR EQUIPMENT RATINGS, SIZES AND FINAL CONFIGURATION.

ISSUE NO.	DATE	W.O.	DESCRIPTION	DWN BY	CKD BY	REVIEWED	APPD
4	2/2024		REVISE DTT SCHEME				
3	1/2023		REMOVE LOR RESET				
2	2/2022		CLARIFICATIONS				
1	9/2020		MINOR REVISIONS				
0	1/2019		ORIGINAL ISSUE				

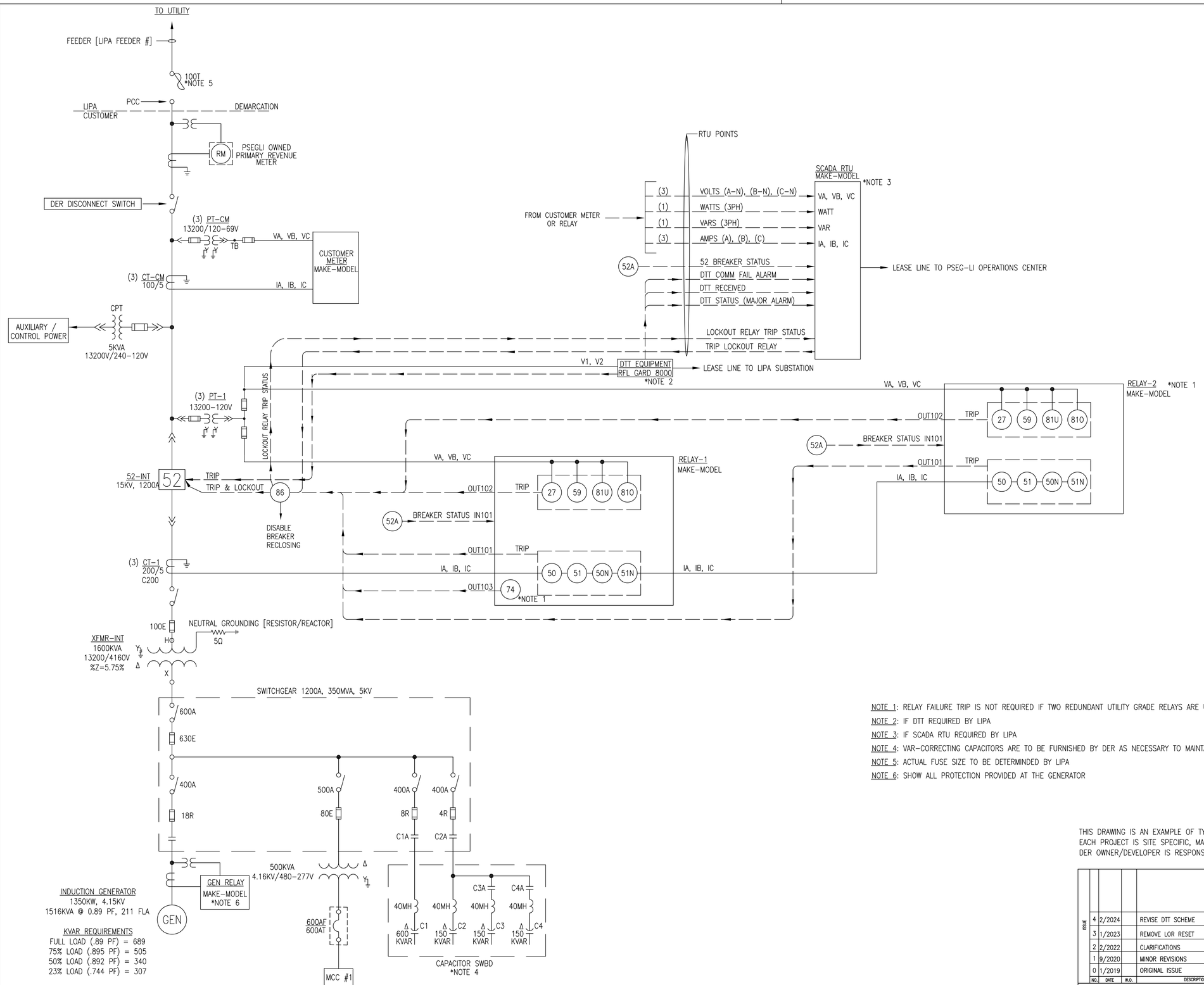
APPENDIX D
SAMPLE DRAWING D-2

FUNCTIONAL DIAGRAM
SYNCHRONOUS GENERATOR DER

PSEG LONG ISLAND

SCALE

VENDOR DWG. NO.



ANSI FUNCTIONS

- 27 UNDERVOLTAGE RELAY
- 50 PHASE INSTANTANENOUS OVERCURRENT RELAY
- 50N GROUND INSTANTANEOUS OVERCURRENT RELAY
- 51 PHASE TIME OVERCURRENT RELAY
- 51N GROUND TIME OVERCURRENT RELAY
- 52 CIRCUIT BREAKER
- 59 OVERVOLTAGE RELAY
- 74 RELAY FAILURE ALARM
- 81 U/O UNDER/OVER FREQUENCY RELAY
- 86 LOCKOUT RELAY (MANUAL RESET)

NOTE 1: RELAY FAILURE TRIP IS NOT REQUIRED IF TWO REDUNDANT UTILITY GRADE RELAYS ARE USED

NOTE 2: IF DTT REQUIRED BY LIPA

NOTE 3: IF SCADA RTU REQUIRED BY LIPA

NOTE 4: VAR-CORRECTING CAPACITORS ARE TO BE FURNISHED BY DER AS NECESSARY TO MAINTAIN NEAR-UNITY SYSTEM POWER FACTOR AND MUST BE REVIEWED AND APPROVED BY PSEGLI

NOTE 5: ACTUAL FUSE SIZE TO BE DETERMINDED BY LIPA

NOTE 6: SHOW ALL PROTECTION PROVIDED AT THE GENERATOR

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DER OWNER/DEVELOPER IS RESPONSIBLE FOR EQUIPMENT RATINGS, SIZES AND FINAL CONFIGURATION.

ISSUE NO.	DATE	W.O.	DESCRIPTION	DWN BY	CKD BY	REVIEWED	APPD
4	2/2024		REVISE DTT SCHEME				
3	1/2023		REMOVE LOR RESET				
2	2/2022		CLARIFICATIONS				
1	9/2020		MINOR REVISIONS				
0	1/2019		ORIGINAL ISSUE				

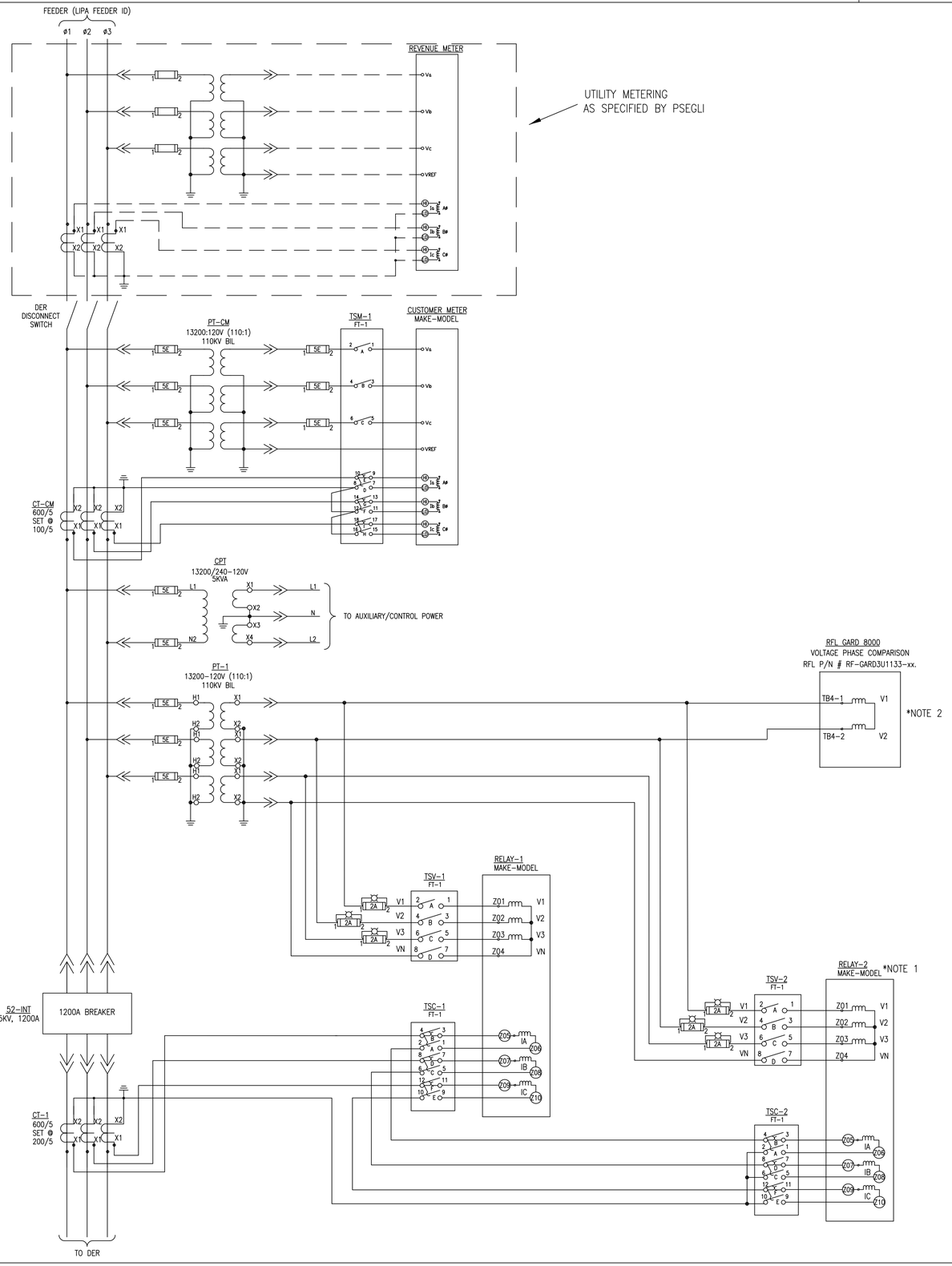
APPENDIX D
SAMPLE DRAWING D-3

FUNCTIONAL DIAGRAM
INDUCTION GENERATOR DER

PSEG LONG ISLAND

SCALE

VENDOR DWG. NO.



NOTE 1: IF USING REDUNDANT UTILITY GRADE RELAY

NOTE 2: 60Hz INPUT VOLTAGE PHASOR MUST MATCH REMOTE END VOLTAGE PHASOR.

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DER OWNER/DEVELOPER IS RESPONSIBLE FOR EQUIPMENT RATINGS, SIZES AND FINAL CONFIGURATION.

ISSUE NO.	DATE	W.O.	DESCRIPTION	DWN BY	CKD BY	REVIEWED	APPD
2	2/2024		ADD DTT SYNC VOLTAGE				
1	9/2020		MINOR REVISIONS				
0	1/2019		ORIGINAL ISSUE				

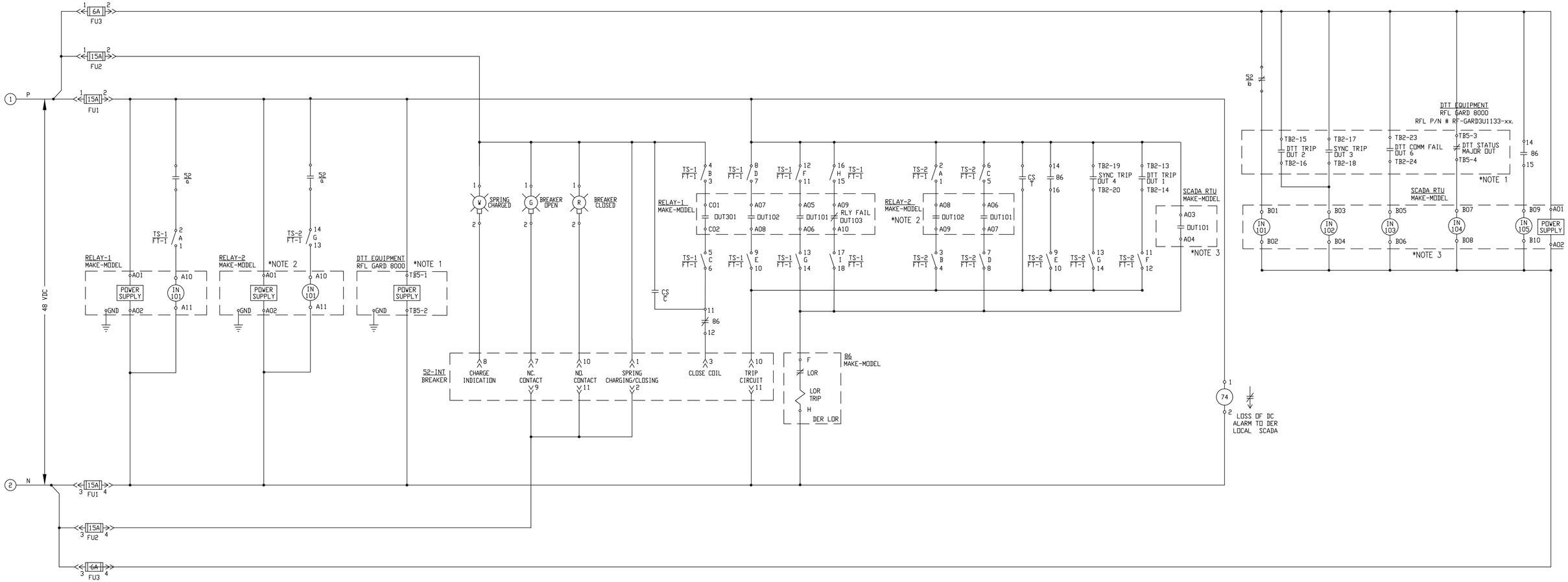
APPENDIX D
SAMPLE DRAWING D-4

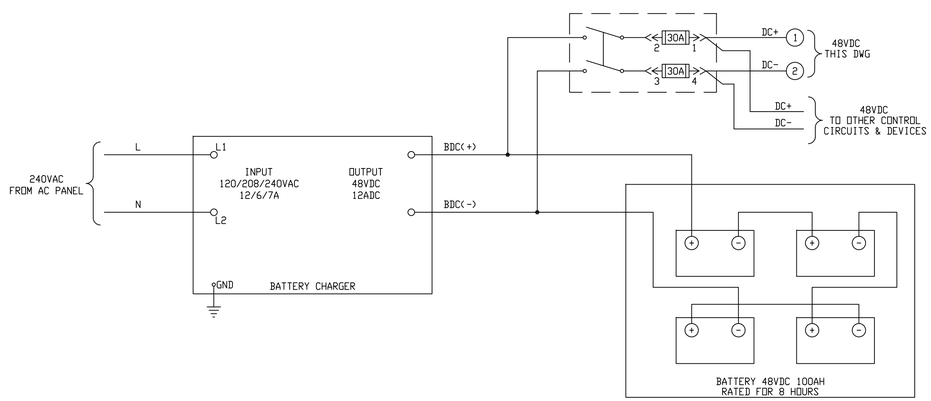
DER THREE LINE DIAGRAM

PSEG LONG ISLAND

SCALE

VENDOR DWG. NO.





NOTE 1: IF DTT REQUIRED BY LIPA
NOTE 2: IF USING REDUNDANT UTILITY GRADE RELAY
NOTE 3: IF SCADA REQUIRED BY LIPA

THIS DRAWING IS AN EXAMPLE OF TYPICAL INTERCONNECTION TO ILLUSTRATE THE TYPE OF INFORMATION TO BE PROVIDED.
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DER OWNER/DEVELOPER IS RESPONSIBLE FOR EQUIPMENT RATINGS, SIZES AND FINAL CONFIGURATION.

ISSUE NO.	DATE	W.O.	DESCRIPTION	DWN BY	CKD BY	REVIEWED	APPD
4	2/2024		ADD DTT SYNC VOLTAGE TRIP				
3	1/2023		REMOVE LOR RESET				
2	2/2022		CLARIFICATIONS				
1	9/2020		MINOR REVISIONS				
0	1/2019		ORIGINAL ISSUE				

APPENDIX D
SAMPLE DRAWING D-5

DC SCHEMATIC FOR DER

PSEG LONG ISLAND

SCALE

VENDOR DWG. NO.